



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,106	12/15/2003	Gerald L. Everett	200315774-1	5509
22879 7590 11/01/2007 HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			EXAMINER CHOI, WOO H	
			ART UNIT 2189	PAPER NUMBER
			MAIL DATE 11/01/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.



UNITED STATES DEPARTMENT OF COMMERCE

**U.S. Patent and Trademark Office**

Address : COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10737106	12/15/03	EVERETT ET AL.	200315774-1

HEWLETT PACKARD COMPANY  
P O BOX 272400, 3404 E. HARMONY ROAD  
INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

**EXAMINER**

Woo H.. Choi

ART UNIT	PAPER
----------	-------

2189

20071028

DATE MAILED:

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner for Patents**

Attached is a revised Examiner's Answer that includes a list of all references relied upon in section 8) Evidence Relied Upon.

  
Woo H. Choi  
Primary Examiner



UNITED STATES PATENT AND TRADEMARK OFFICE

---

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/737,106  
Filing Date: December 15, 2003  
Appellant(s): EVERETT ET AL.

**MAILED**

**NOV 01 2007**

**Technology Center 2100**

---

Joel D. Youngs  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed July 2, 2007 appealing from the Office action mailed October 18, 2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is incorrect. The Brief states that claims 1 – 24 stand rejected. Appellant presented claims 1 – 25 and all claims stand rejected.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

US 2004/0123092	Cepulis et al.	6-2004
US 6,611,912	Maleck et al.	8-2003
US 6,199,159	Fish	3-2001

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 112***

1. Claims 2 – 4 and rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation “said system call requesting said memory allocation”.

There is insufficient antecedent basis for this limitation in the claim. It is also not clear whether “said system call” is for one memory allocation or three separate allocations. Claims 3 and 4 are rejected for containing the deficiency of the parent claim as discussed above.

***Claim Rejections - 35 USC § 102***

2. Claims 1 – 3, 8 – 14, 18 – 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Cepulis et al. (US Patent Application Publication No. 2004/0123092, hereinafter “Cepulis”).

3. With respect to claims 1, 2, 8 – 14 and 18 – 22, Cepulis discloses a computer implemented method for establishing a run-time data area comprising:

**relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation** (figure 2, page 3, paragraph 16, figure 2 shows a flow diagram of a boot process where PAL and SAL BIOS ROM procedures are executed; pages 3-4, paragraph 19, “In order to facilitate efficient reading and execution of the PAL and SAL routines, embodiments of this invention copy or shadow the PAL and SAL routines to a shadow area of the main memory array.”; the Examiner notes that Appellant’s use of the word “relocating” is somewhat misleading because while a firmware module can be copied onto a writeable area and executed, it cannot be moved to a writeable area);

**reserving a portion of said writeable memory location comprising a memory allocation for said firmware module and an additional memory allocation** (Figure 3, 58, explicitly shows area reserved for the firmware module; paragraph [21] “the PAL abstraction layer and SAL abstraction layer may implement *spinlocks* with respect to each operating system to ensure that, as between the two (or more) operating systems, a second call to a non-reentrant PAL and SAL routine is not allowed until a previously called instance of the same routine runs to completion”; spinlocks are locks or semaphores used to control access to shared resources and they require memory space to hold state or status of locks); **and**

**designating said additional memory allocation as said run-time data area, wherein said run-time data area is created without requiring prior knowledge of system resource allocation** (memory area containing spinlocks is a run-time data area because it is used at run-time by programs accessing PAL and SAL routines and allocation of this area does not require prior knowledge of system resource allocations, for example, resources allocated for I/O ports, peripherals, etc.).

Receiving memory allocation calls and returning responses to memory allocation responses are part of normal operation of any memory management system. This teaching is implicit in Figure 3, which shows actual allocation and occupation of the allocated memory space by the PAL and SAL modules.

Claims 8 and 18 claim memory allocation steps required to perform the relocation function claimed in claim 1, without reciting actual "relocation" steps. As shown above, Cepulis discloses actual relocation, or copying of the BIOS ROM (system firmware) onto the shadow area 58 of the main memory array 18, as claimed in claim 1. Determining the size of an object to be copied to a memory area is a necessary step in a copying operation as the system must know how much space to allocate and how many bytes to transfer. Allocation or reservation of space is also required to 1) determine where to copy the firmware, 2) to prevent other programs from overwriting this region and 3) to prevent the firmware copying process from overwriting memory locations reserved for other functions. Figure 3 explicitly shows the area reserved for PAL and SAL.

As to “intercepting” and “receiving a system call” limitations, computer programs are organized as a collection of modules known by various names in the art such as routines, procedures, functions, sub-programs, etc. (see for example, figure 3, PAL and SAL comprises multiple modules or routines; PAL abstraction 80 “intercepts” or “receives” calls directed to modules; PAL modules also “receives” or “intercepts” calls). These modules are “called” to perform their respective functions. The called module “receives” or “intercepts” the call.

4. With respect to claims 3, 4, 8 – 14, see figures 1 and 3, allocating shadow to load PAL and SAL routines require knowledge of sizes of routines. Likewise, the spin lock variable storage size must be known for proper reading and writing of the variable.

5. With respect to claim 21, see figure 3.

6. Claims 1, 8, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Malek et al. (US Patent No. 6,611,912, hereinafter “Malek”).

7. With respect to claim 1, Malek discloses a method for creating a system independent run-time data storage area comprising:

relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up process (see figure 2 and figure 4, 404, a firmware module in EEPROM 201 is relocated to a writeable memory location in the system RAM; col. 3, line 61 –



col. 4, line 6; col. 4, lines 25 – 29; Malek's invention is directed to enumeration and configuration of devices during a system startup, i.e., boot-up process);

reserving a portion of said writeable memory location comprising a memory allocation for said firmware module and an additional memory allocation (see figure 2);

designating said additional memory allocation as said run-time data area, wherein said run-time data area is created without requiring prior knowledge of system resource allocation (areas other than Add-on ROM are available for run-time data and run-time programs, see also 301, 302, and 406, these areas contain hardware configuration data required at run-time; prior knowledge of system resource allocation such as allocation of software device drivers, allocation of memory space for application programs, for example, are not required at this point as these resources are loaded or determined later in the operating system boot process).

8. As to claims 8 and 18, see discussion of these claims above. Just as in Cepulis, Malek discloses actual relocation of an EEPROM firmware to system main memory (figure 2).

### ***Claim Rejections - 35 USC § 103***

9. Claims 5 – 7, 15 – 17 and 23 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malek in view of Fish (US Patent No. 6,199,159).

Malek discloses all of the limitations of the parent claims as discussed above. However, Malek does not specifically disclose that the firmware module operates in real mode and virtual mode. On the other hand, Fish discloses a computer system that operates in real mode (Fish, Figure 4, 66, 68; see also abstract) and virtual mode (Figure 4, 70). It would have been obvious

to one of ordinary skill in the art, having the teachings of Malek and Fish before him at the time the invention was made, to operate the Malek's firmware module in real mode and virtual mode as taught by Fish to make the system backward compatible (Fish, col. 1, lines 56 – 60). Fish discloses that some real mode programs still require execution in the real mode (col. 1, lines 16 – 22). Fish further discloses that there exists a continuing need for a mechanism to use a real mode operating system in conjunction with a virtual mode operating system when the BIOS does not support booting up the real mode operating system (col. 1, lines 56 – 60).

#### **(10) Response to Argument**

##### **Indefiniteness**

Appellant merely alleges that there is sufficient antecedent basis without providing any real argument. While the claim recites the limitation “a system call for a system firmware feature” in claim 2, this system call for a system firmware feature is not a proper antecedent basis for a specific “system call for requesting said memory allocation for said firmware module.” The claim does not recite any act or step of requesting memory allocation for the firmware module with a system call. The limitation mentions three distinct areas for allocation, one for said firmware module, one for said additional memory, and for said system firmware feature. The claim itself makes it clear that a memory allocation for the firmware module is not the same as a memory allocation for the system firmware feature. While there is an antecedent basis for a generic system call for a system firmware feature (which can be a call for any system feature), there is no specific system call for any memory allocation. Even assuming that a generic system call for a system firmware feature can be construed as a specific system call for memory

allocation, a reasonable interpretation of the limitation would be for memory allocation for the system firmware feature. The claim recites no system call for memory allocation for the firmware module, which is distinct from the system firmware feature memory.

It is also not clear whether there is to be one request and one response or three separate requests and responses for an allocation of memory for the firmware module, an additional memory allocation, and a memory allocation for system firmware feature.

Appellant can easily overcome this rejection by further limiting “a system call for a system firmware feature” to recite memory allocation (for example, “a system call for allocation of memory areas for the firmware module, the additional memory and the system firmware feature” or “system calls for allocation of memory areas for ..., respectively”).

#### **Anticipation by Cepulis**

Appellant's only disagreement with the Examiner is the limitation “relocating a firmware module from a read-only memory location to a writeable memory location during a system boot-up operation,” as claimed in independent claim 1. Appellant cites a portion of a single sentence in paragraph 17 of Cepulis (“the computer system may have the capability of logically partitioning the computer resources and then executing multiple operating systems, one in each partition”) that is unrelated to the claimed limitation and concludes that this is different from the disputed limitation. The Examiner agrees that the passage Appellant cited from Cepulis is different from the claimed limitation. The Examiner also agrees that the cited passage does not teach the disputed limitation. However, the Examiner does not understand how “proving” (by

citing a passage that is unrelated to the claimed limitation, and not relied upon by the Examiner in the rejection) that Cepulis teaches something in addition to what Appellant claimed proves that Cepulis does not teach the limitation in dispute.

As discussed above, Appellant's claimed "relocation" of firmware to a writeable memory location is actually copying of the code in ROM to RAM and executing the code in RAM (see Specification, figure 2A). By definition, a piece of ROM code cannot be moved without physically removing the ROM chip. It can only be copied. Cepulis' teaching of "shadowing" or copying the ROM code to the main memory and executing the code from the memory corresponds exactly to what Appellant claims by "relocation" of ROM to a writeable memory. Cepulis also discloses that PAL and SAL ROM codes are executed during boot-up process and are available after the boot-up process as well (paragraph 19).

### **Anticipation by Malek**

Appellant specifically argues that "[w]ith the present invention, the firmware is relocated and not shadowed, as with Malek" without showing a patentable difference between the two acts. As discussed above, Appellant's "relocating" is copying of ROM code to a writeable location (see Appellant's specification, figure 2A) just as Malek's "shadowing" is (see Malek, figure 2). As shown in figure 2, "shadowing" is copying of EEPROM code to system RAM for execution in RAM. Appellant's use of different words to claim acts known in the prior art does not make the claims patentable.

### **Obviousness**

Appellant merely repeats the same allegation against Malek regarding “relocating a firmware module ...” without presenting any new argument. As discussed above, Malek discloses “relocating”. Therefore, Appellant has not rebutted the prima facie case of obviousness of claims 5 – 7, 15 – 17 and 23 – 25 under USC 103(a).

The Examiner notes that Appellant states, at page 14, line 2, of the Brief that claims 1 – 30 are rejected (as opposed to claims 1 – 24 as stated in the status of the claims section of the Brief). Again, this is incorrect. There are only 25 claims. All claims, 1 – 25, are rejected.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner’s answer.

Art Unit: 2189

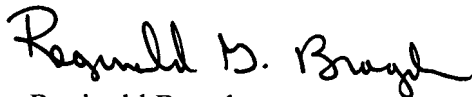
For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



Woo H. Choi  
Primary Examiner  
GAU 2189

Conferees:



Reginald Bragdon  
Supervisory Patent Examiner  
GAU 2189

Donald Sparks  
Supervisory Patent Examiner  
GAU 2187



**DONALD SPARKS**  
**SUPERVISORY PATENT EXAMINER**